Docket No.: P2001,0373

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant

JUDITH MAGET

Filed -

CONCURRENTLY HEREWITH

Title

INTEGRATED, TUNABLE CAPACITANCE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

- U.S. Patent No. 6,172,378 B1 (Hull et al.), dated January 9, 2001;
- U.S. Patent No. 5,965,912 (Stolfa et al.), dated October 12, 1999;
- U.S. Patent No. 6,034,388 (Brown et al.), dated March 7, 2000;

Patent Abstracts of Japan 03147376 A (Hidetomo), dated June 24, 1991;

European Patent Application EP 0 800 218 A2 (McFarland et al.), dated October 8, 1997;

Hung, C.-M. et al.: "A 25.9-GHz Voltage-Controlled Oscillator Fabricated in a CMOS Process", Symposium on VLSI Circuits Digest of Technical Papers, IEEE, 2000, pp. 100-101;

Maget, J. et al.: "A Varactor with High Capacitance Tuning Range in Standard 0.25µm CMOS Technology", 4 pages;

Burghartz, J. N. et al.: "Integrated RF and Microwave Components in BiCMOS Technology", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1559-1570;

Wong, W. M. Y. et al.: "A Wide Tuning Range Gated Varactor", IEEE Journal of Solid-State Circuits, Vol. 35, No. 5, May 2000, pp. 773-779;

Svelto, F. et al.: "A Three Terminal Varactor for RF IC's in Standard CMOS Technology", IEEE Transactions on Electron Devices, Vol. 47, No. 4, April 2000, pp. 893-895;

Tiebout, M.: "A Fully Integrated 1.3GHz VCO for GSM in 0.25µm Standard CMOS with a Phasenoise of –142dBc/Hz at 3MHz Offset", European Microwave Week, 2000, 4 pages;

Andreani, P. et al.: "On the Use of MOS Varactors in RF VCO's", IEEE Journal of Solid-State Circuits, Vol. 35, No. 6, June 2000, pp. 905-910;

Porret, A.-S. et al.: "Design of High-Q Varactors for Low-Power Wireless Applications Using a Standard CMOS Process", IEEE Journal of Solid-State Circuits, Vol. 35, No. 3, March 2000, pp. 337-345;

International Search Report, dated December 4, 2002.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant. As per the Notice in 1273 OG 55 (August 5, 2003) no copies of any above-mentioned U.S. patents and U.S. patent application publications are submitted for any application filed after June 30, 2003.

Respectfully submitted

LAURENCE A. GREENBERG REG. NO. 29,308

For Applicant

ປົate: November 13, 2003

Lerner and Greenberg, P.A. Post Office Box 2480 Hollywood, FL 33022-2480

Tel: (954) 925-1100 Fax: (954) 925-1101

/nt/kf

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))				Appl. No.:					
				Applicant: JUDITH MAGET Filing Date: November 13, 2003 Group Art Unit:					
							•		
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS		ING TE	
WWW.CO	Α	6,172,378 B1	1/9/01	Hull et al.	02,100	027.00			
	В	5,965,912	10/12/99	Stolfa et al.					
	c	6,034,388	3/7/00	Brown et al.					
	D								
	E								
	F								
	G			·					
	Н	·						·	
	1	·							
		FOREIG	GN PATEN	NT DOCUMENT				:	
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRAI YES		
	J	03147376 A	6/24/91	Japan					
	K	0 800 218	10/8/97	Europe					
	L								
	М								
	N					-			
отн	ER D	OCUMENTS (Incl	uding Auth	nor, Title, Date, Pe	rtinent Pa	iges, etc.)		
		CMOS Process", S IEEE, 2000, pp. 10	Symposium 00-101	Hz Voltage-Controlle on VLSI Circuits Di	gest of Te	chnical Pa	apers,		
		Maget, J. et al.: "A 0.25 µm CMOS Te		vith High Capacitand 4 pages	e Tuning	Range in	Standa	ard	
EXAMINER				DATE CONSIDERED					
•				DATE CONSIDE					

FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			Attorney Docket No.: P2001,0373 Appl. No.: Applicant: JUDITH MAGET Filing Date: November 13, 2003 Group Art Unit:					
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))								
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS		ING TE
	Α							
	В			,				
	С							
	D			·				
	E							
	F							
	G							
	Н							
	1		,					
		FOREIC	ON PATE	NT DOCUMENT				
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRA YES	
	J							
	K							
	L							
	М							
-	N							
ОТН	ER DO	OCUMENTS (Inclu	ıding Aut	hor, Title, Date, Pe	rtinent Pa	ges, etc.)	
		Burghartz, J. N. et al.: "Integrated RF and Microwave Components in BiCMOS Technology", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1559-1570					ios	
		Wong, W. M. Y. et	al.: "A Wi	de Tuning Range Ga No. 5, May 2000, pp		tor", IEEE	Journ	al of
EXAMINER				DATE CONSIDERED				
			-	vhether or not cita				
				if not in conformatication to application to		not con	sider	ea.
morade copy	Or tri	O JOHN WILLI HEAL	Sommul	modition to applice	.,			

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			Attorney Docket No.: P2001,0373 Appl. No.: Applicant: JUDITH MAGET Filing Date: November 13, 2003 Group Art Unit:					
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))								
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS		ING ATE
	Α							
	В							
	С							
	D				-	·		
	E							
	F						ļ <u>.</u>	
	<u>G</u>		-					
	H							
		<u> </u>]					
		FOREIG	GN PATE	NT DOCUMENT				
		TORLA		THE BOOK INC.				
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRA YES	NSL. NO
	J			1	CLASS			
	J			1	CLASS			
	 			1	CLASS			
	К			1	CLASS			
	K			1	CLASS			
ОТН	K L M		DATE	COUNTRY		CLASS	YES	
ОТН	K L M	DOCUMENT NO. OCUMENTS (Inclusive Andrews Andr	DATE uding Aut	country nor, Title, Date, Perminal Varactor for frons on Electron De	ertinent Pa	ages, etc.) CMOS April	NO
· -	K L M	DOCUMENT NO. OCUMENTS (Inclusive Svelto, F. et al.: "A Technology", IEEE 2000, pp. 893-895 Tiebout, M.: "A Fu	DATE Uding Authorized Transact Ily Integrate senoise of	country country nor, Title, Date, Perminal Varactor for from on Electron Derect 1.3GHz VCO for -142dBc/Hz at 3MHz ages	ertinent Pa RF IC's in S vices, Vol. GSM in 0.: Iz Offset",	ages, etc. Standard C 47, No. 4,	YES) CMOS April	NO
OTH	K L M	DOCUMENT NO. OCUMENTS (Inclusive Svelto, F. et al.: "A Technology", IEEE 2000, pp. 893-895 Tiebout, M.: "A Ful CMOS with a Phase	DATE Uding Authorized Transact Ily Integrate senoise of	country country nor, Title, Date, Perminal Varactor for Fons on Electron Development 1.3GHz VCO for –142dBc/Hz at 3MHz	ertinent Pa RF IC's in S vices, Vol. GSM in 0.: Iz Offset",	ages, etc. Standard C 47, No. 4,	YES) CMOS April	NO
EXAMINER EXAMINER:	K L M N ER D	DOCUMENT NO. OCUMENTS (Inclusive Svelto, F. et al.: "A Technology", IEEE 2000, pp. 893-895 Tiebout, M.: "A Ful CMOS with a Phase	DATE DATE Uding Aut Three Te Transact Ily Integrat senoise of 2000, 4 pa	country country country con, Title, Date, Perminal Varactor for from on Electron Derection De	ertinent Parent	eges, etc. Standard (47, No. 4, 25µm Star European) CMOS April ndard	NO NO

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))			Attorney Docket No.: P2001,0373 Appl. No.: Applicant: JUDITH MAGET Filing Date: November 13, 2003 Group Art Unit:													
								EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	i	ING TE
	Α															
	В							-								
	С															
	D															
	E															
	F															
	G				<u> </u>			•								
	Н															
				<u> </u>	<u></u>											
		FOREIC	SN PATE	NT DOCUMENT	• .											
		I				SUB	TRA									
		DOCUMENT NO.	DATE	COUNTRY	CLASS	CLASS	YES	TINO								
	J	DOCUMENT NO.	DATE	COUNTRY	CLASS	CLASS	YES	INC								
	J K	DOCUMENT NO.	DATE	COUNTRY	CLASS	CLASS	YES	INO								
	-	DOCUMENT NO.	DATE	COUNTRY	CLASS	CLASS	YES	INO								
	K L M	DOCUMENT NO.	DATE	COUNTRY	CLASS	CLASS	YES	INO								
	K L	DOCUMENT NO.	DATE	COUNTRY	CLASS	CLASS	YES	INO								
ОТН	K L M			COUNTRY hor, Title, Date, Pe				INO								
ОТН	K L M	OCUMENTS (Inclu	uding Aut		ertinent Pars in RF V0	ages, etc.)									
ОТН	K L M	Andreani, P. et al.: of Solid-State Circ Porret, AS. et al.: Applications Using	uding Aut "On the Uuits, Vol. 3 "Design of	hor, Title, Date, Pe Use of MOS Varacto 15, No. 6, June 2000 of High-Q Varactors rd CMOS Process",	ertinent Pars in RF VO p, pp. 905-9 for Low-Po IEEE Journ	ages, etc. CO's", IEE 010 ower Wirel) E Jou	rnal								
OTH	K L M	Andreani, P. et al.: of Solid-State Circ Porret, AS. et al.: Applications Using	uding Aut "On the Luits, Vol. 3 "Design of a Standa	hor, Title, Date, Pe Use of MOS Varacto 15, No. 6, June 2000 of High-Q Varactors	ertinent Pars in RF VO 1, pp. 905-9 for Low-Po IEEE Journ	ages, etc. CO's", IEE 010 ower Wirel) E Jou	rnal								
EXAMINER	K L M N ER D	Andreani, P. et al.: of Solid-State Circ Porret, AS. et al.: Applications Using Circuits, Vol. 35, N	uding Aut "On the Luits, Vol. 3 "Design of a Standard of Standar	hor, Title, Date, Person of High-Q Varactors of CMOS Process, th 2000, pp. 337-345	ertinent Pars in RF VO 1, pp. 905-9 for Low-Po IEEE Journ 5 ERED	ages, etc. CO's", IEE 010 ower Wirel nal of Soli) E Jou ess d-Stat	rnal								
EXAMINER: with MPEP 6	M N ER DO	Andreani, P. et al.: of Solid-State Circ Porret, AS. et al.: Applications Using Circuits, Vol. 35, N	uding Aut "On the Uuits, Vol. 3 "Design of a Standardon 3, Marco	bor, Title, Date, Person of MOS Varactors of High-Q Varactors of CMOS Process, the 2000, pp. 337-345 DATE CONSID	ertinent Pars in RF V0, pp. 905-9 for Low-Por IEEE Journs ERED ation is in ance and	ages, etc. CO's", IEE 210 ower Wirel nal of Soli	ess d-Stat	rnal								